

## Research Article

# Design and Simulation of a Fully Digitized GNSS Receiver Front-End

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In the near future, RF front-ends of GNSS receivers may become very complicated when multifrequency signals are available from at least four global navigation systems. Based on the direct RF sampling technique, fully digitized receiver front-ends may solve the problem. In this paper, a direct digitization RF front-end scheme is presented. At first, a simplified sampling rate selection method is adopted to determine the optimal value. Then, the entire spectrum of GNSS signal is directly digitized through RF sampling at a very fast sampling rate. After that, the decimation and filtering network is designed to lower the sampling rate efficiently. It also realizes the digital downconversion of the signal of interest and the separation of narrow band signals from different navigation systems. The scheme can be flexibly implemented in software. Its effectiveness is proved through the experiment using simulated and true signals.

## 1. Introduction

With the development of global navigation satellite system (GNSS) including GPS, GLONASS, GALILEO, and COMPASS, multi-constellation signals will be available in the future. These signals mainly concentrate in 1164~1300 MHz and 1559~1610 MHz (referred as "Band I" and "Band II" below). In order to receive all of the GNSS signals, conventional RF front-end may not fit for future multisystem receivers. From the theory of software radio, A/D needs to be set as close to the antenna as possible, thus a single hardware configuration could operate as multiple receivers simply by changing the software programming [1]. Based on such idea, the direct RF sampling offers several advantages for GNSS RF front-end design. First, it reduces the parts count and eliminates the need to design and fabricate a mixing chip with a specially tailored frequency plan. Second, it simplifies the design of new receivers for the new signals that will become available as GPS gets modernized and as Galileo comes on line. Third, it is possible to make a single RF front-end for multiple frequency bands.

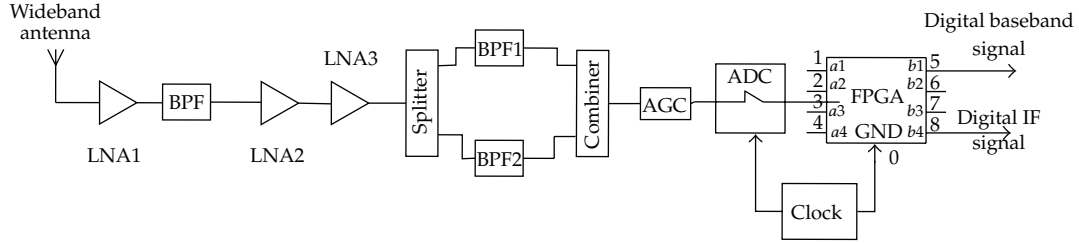


Figure 1: Block diagram of the direct RF sampling system.

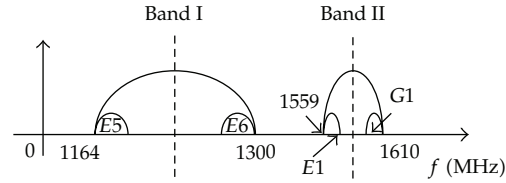


Figure 2: Frequency spectrum of Band I and II.

This approach to multifrequency GNSS receiver front-end design eliminates the need for multiple front-ends, which reduces the parts count and eliminates some potential sources of inter channel line bias. Therefore, the digitized RF front-end is becoming a hot research area.

Although software radio is not a novel concept, most studies on direct RF sampling nowadays are still conducted in labs. Brown and Wolt [2] are the first to report on the use of direct RF sampling for the design of GPS receiver front-ends. They concentrated on a system that used a very fast sampling rate, 800 MHz. This system captured the entire spectrum from L2 at 1227.6 MHz up to L1 at 1575.42 MHz in a single information bandwidth centered at 1400 MHz. But their paper presented no experimental results for actual GPS signals. Akos and Tsui [3] and Psiaki et al. [4] developed a method for designing direct RF sampling front-ends for multiple frequency bands, and they tested their method using a signal prototype direct RF-sampling front-end. It is proved that the direct RF sampling is feasible for GNSS receiver front-ends. In China, efforts in direct RF sampling include the work of [5–7].

The studies above mainly focus on the sampling of the one or two narrow band signal, three at most. Differently, our work aims at sampling the entire spectrum of navigation signals: Band I and II. Due to the large bandwidth, the ADC has to work at a very fast sampling rate. Thus, a decimation and filtering network is designed to lower the sampling rate. The network can be realized in field programmable grid array (FPGA), so it is easy to debug and upgrade and convenient for the IC implementation.

## 2. System Framework

Figure 1 shows the block diagram of the direct RF sampling system. GNSS signals are received by a wideband antenna (3 dB band range 1.15~1.65 GHz). Before fed into ADC, they are amplified and filtered in several stages. Afterwards signals out of Band I and II are negligible, as shown in Figure 2. Assuming the ADC specially designed for the RF sampling operating at a very fast rate  $f_s$  in general, it outputs data at the clock rate  $f_s/2$  or  $f_s/4$ . That is

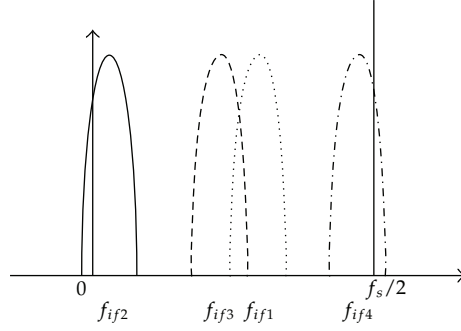


Figure 3: Signal overlap in the Nyquist spectrum due to bad choice of the sampling rate [4].

because high rate data is ordinarily too difficult to deal with. A proper sampling rate should be chosen to prevent the band overlapping. Digitized signals are passed through a decimation and filtering network to lower the sampling rate to an acceptable level. The network also realizes the digital downconversion and separation of the target navigation signal. If only one or two narrow band signal exists, the sampling rate could be very low [3]. Therefore, it is not necessary to add the decimation and filtering network to the system. And the digitized signals can be directly utilized.

In this paper, the analog-based hardware issues in front of the ADC will not be discussed. It is assumed that the signal power, the dynamic range, the input bandwidth and so forth meet the demands of the ADC chipset. How to select a sampling rate properly as well as the design of the decimation and filtering network is of our primary concern.

### 3. Sampling Rate Selection

According to the theory in [4], assuming that one signal contains  $M$  different frequency bands of interest with nominal carrier frequencies of  $f_{cj}$  for  $j = 1, \dots, M$ . The  $j$ th band is sampled to IF  $\bar{f}_{ifj}$  at the rate  $f_s$

$$\bar{f}_{ifj} = \bar{f}_{ifj}(f_s) = f_{cj} - f_s \cdot \text{round}\left(\frac{f_{cj}}{f_s}\right), \quad j = 1, \dots, M, \quad (3.1)$$

where the  $\text{round}()$  function rounds its input argument to the nearest integer. These intermediate frequencies can fall anywhere between  $-f_s/2$  and  $+f_s/2$ . Aliasing to a negative intermediate frequency is analogous to high-side superheterodyne mixing. It is helpful for purposes of receiver design also to define the strictly positive intermediate frequency  $f_{ifj}(f_s) = |\bar{f}_{ifj}(f_s)|$ .

A poor choice of sampling frequency might give rise to the aliased signal structure shown in Figure 3. There are three deficits of this design: (1) The frequency band centered at  $f_{if2}$  overlaps zero, (2) the frequency bands centered at  $f_{if3}$  and  $f_{if1}$  overlap each other, and (3) the frequency band centered at  $f_{if4}$  overlaps the aliasing frequency  $f_s/2$ .

In order to keep the sampled signals from overlapping, there are three constraints corresponding to each deficit mentioned above:

$$a_j(f_s) = \frac{f_{ifj}(f_s)}{B_j/2} \geq 1, \quad (3.2a)$$

$$b_j(f_s) = \frac{f_s/2 - f_{ifj}(f_s)}{B_j/2} \geq 1, \quad (3.2b)$$

$$c_{j,k}(f_s) = \frac{|f_{ifj}(f_s) - f_{ifk}(f_s)|}{B_j/2 + B_k/2} \geq 1, \quad (3.2c)$$

where  $j = 1, \dots, M$ ,  $k = (j + 1), \dots, M$ .  $B_j$  is the bandwidth of the  $j$ th signal. Then  $d(f_s)$  is defined as

$$d(f_s) = \min[a_1(f_s), \dots, a_M(f_s), b_1(f_s), \dots, b_M(f_s), c_{12}(f_s), c_{13}(f_s), \dots, c_{M-1,M}(f_s)]. \quad (3.3)$$

Given this function, the set of acceptable sampling frequencies is  $\{f_s : d(f_s) \geq 1\}$ .

In [4], a complicated algorithm is introduced to calculate the sampling rate in which the break points of  $d(f_s)$  need to be determined. An easier method is adopted in this paper.

The range of  $f_s$  is constrained by

$$f_s \geq \sum_{j=1}^M B_j, \quad (3.4)$$

$$f_s \leq 2 \cdot \max(f_{c_j}).$$

The function  $d(f_s)$  can be coarsely plotted in Matlab if the step rate of the variable  $f_s$  is small. And all the  $f_s$  values that satisfy the limit:  $\{f_s : d(f_s) \geq 1\}$  are saved in a file. Considering the situation in Figure 2, Band I is centered at 1.232 G with bandwidth 136 MHz and Band II at 1.5845 G with bandwidth 51 MHz. Thus,  $M = 2$ . The function  $d(f_s)$  is drawn in Figure 4. From the recorded values, the minimal acceptable sampling rate is about 536 MHz. However, 744 MHz is chosen as the system sampling rate which obviously satisfies the limit as demonstrated in Figure 4. Another reason for such choice is that it is convenient for the performance comparison between the direct RF sampling system and the analog RF front-end which has already been used in our receiver.

#### 4. Decimation and Filtering Network

From the analysis above, sampling Band I and II at 744 MHz will not lead to overlapping over each other. The frequency spectrum after sampling is shown in Figure 5. For GPS L1 within Band II, the lowest aliased intermediate equivalent of the original RF carrier frequency 1575.42 MHz is 87.42 MHz. Due to the fact that data at the high sampling rate like 744 MHz is difficult for most digital processors nowadays to deal with, the rate has to be lowered. Another objective is to separate the signal of a specific satellite system from the entire information band of Band I or II. As a result, it can be used by a single-system receiver.

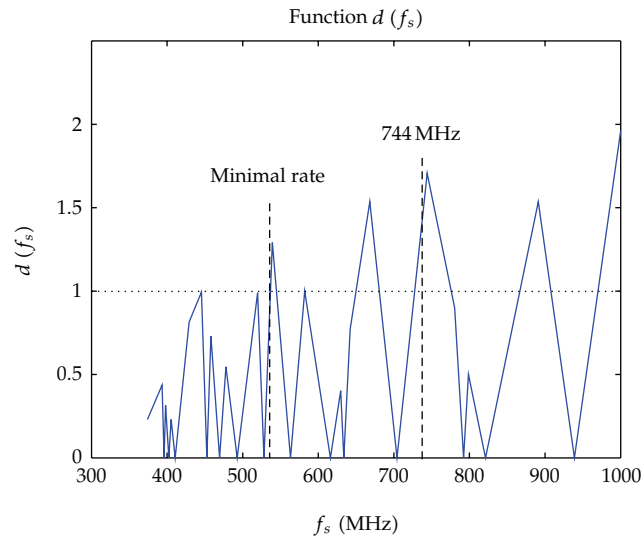


Figure 4: A portion of function  $d(f_s)$  for Band I and II.

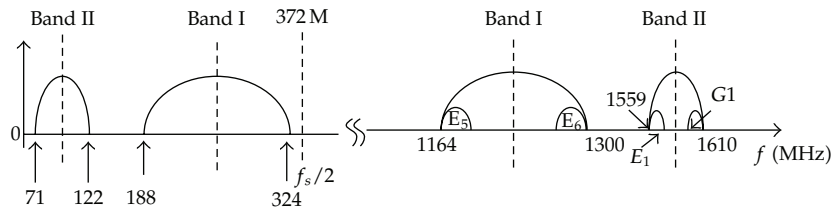
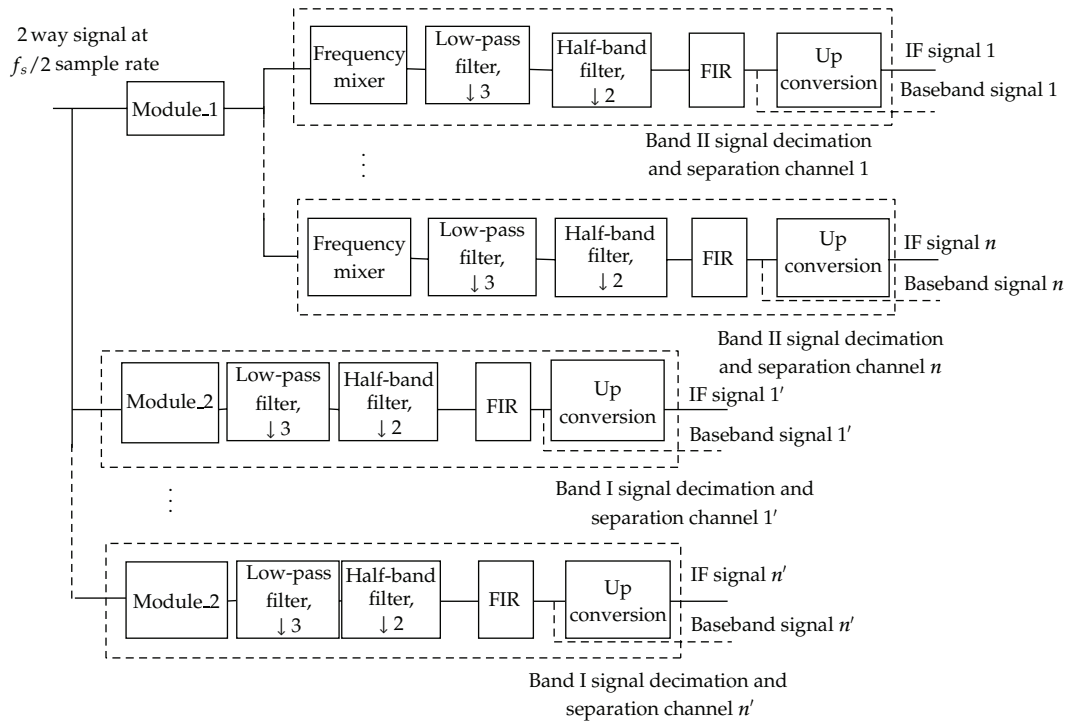


Figure 5: Signal frequency spectrum after bandpass sampling of Band I and II.

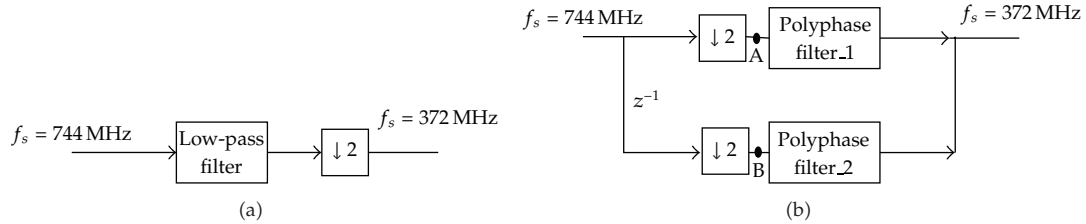
Therefore, based on the multirate signal processing theory [8], a decimation and filtering network is designed to solve the problem. The target clock rate is 62 MHz, thus the overall decimation factor is 12 and the sampling rate reduction occurs in a series of 3 stages:  $2 \times 3 \times 2$ .

The structure of the decimation and filtering network is shown in Figure 6. Module\_1 in this figure is for directly decimating Band II signals by the factor 2 after filtering Band I signals out of the ADC output. The block diagram of Module\_1 is illustrated in Figure 7. From the spectrum depicted in Figure 5, only a low-pass filter in Figure 7(a) is needed to eliminate the Band I. It is very difficult to design a low-pass filter at the sampling rate of 744 MHz. So, an equivalent structure in Figure 7(b) is adopted. The low-pass filter is implemented using the polyphase structure. With decimators set in front, the filtering is performed at the lower sampling rate. Thus, it becomes an efficient structure. Commonly, the ADC chipsets specially designed for direct RF sampling can provide two way outputs each at half-sampling rate [9]. The timing of the ADC output is same as that of point A and B in Figure 7. Due to such characteristic of the ADC, the decimation by the factor 2 is chosen as the first stage. Saving two decimators, Module\_1 is just composed of two poly-phase filters.

Filtered by Module\_1, only entire Band II signal at the clock rate of 372 MHz is left to deal with. It is input into a processing branch named as “Band II signal decimation and separation channel”, in which the signal of a certain navigation system is decimated by the factor 6 and separated from Band II. At first, a frequency mixer is used to down convert the



**Figure 6:** The structure of the decimation and filtering network.



**Figure 7:** The block diagram of Module.1.

signal of interest centered at one frequency to the baseband (I and Q). The following low-pass filter serves as the anti alias filter for the next stage decimation while restraining the out-of-band noise as much as possible. The Half-band decimator is chosen for the last stage decimation by the factor 2. At last, a FIR low-pass filter eliminates out-of-band noise further and compensates the transfer function of total decimation filters.

Concerning the interested signal within Band I, the separation strategy is slightly different. The decimation by the factor 2 is completed by Module.2. Figure 8 is the block diagram of Module.2. In Figure 8(a), the signal of interest is down converted to the baseband firstly. Then, it is passed through a low-pass filter which excludes out-of-band noise and limits the bandwidth for the decimator followed. Similar to Module.1, the frequency mixer and filtering should be put behind the decimator to come into an efficient structure illustrated in Figure 8(c), which is equal to the one in Figures 8(a) and 8(b). The two-way output of the ADC can also be used to point A and B like the situation in Figure 7(b). The principle of the

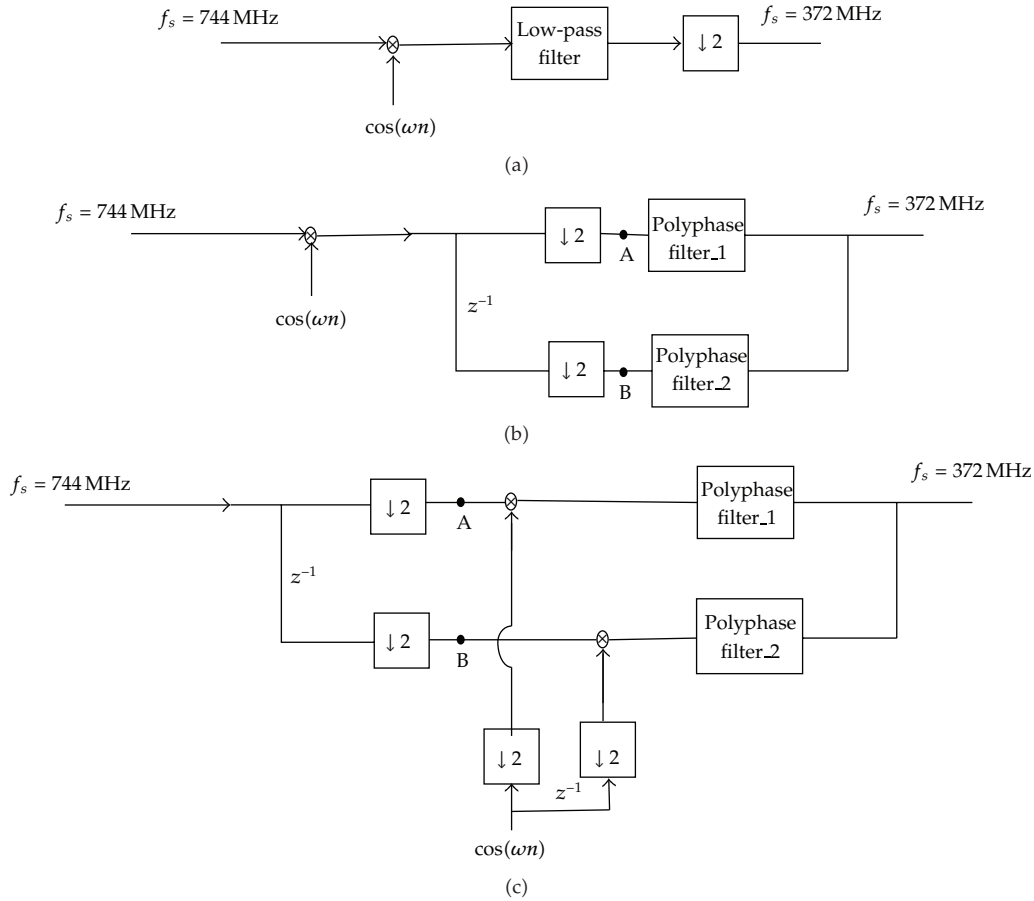


Figure 8: The block diagram of Module 2.

rest of “Band I signal decimation and separation channel” is analogous to that of Band II, thus it will not be elaborated repeatedly.

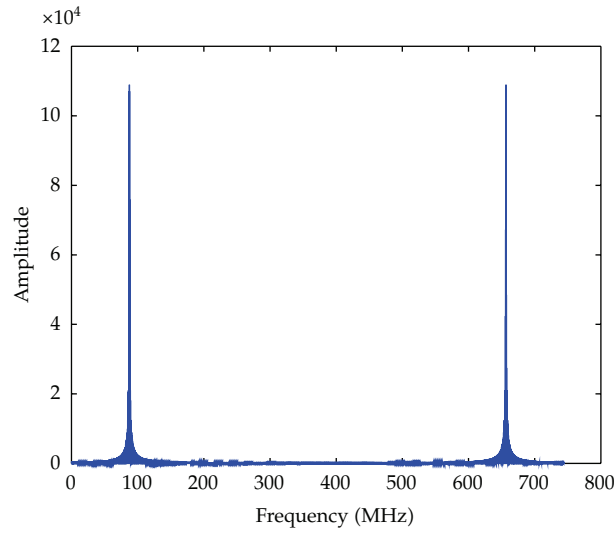
## 5. Experimental Results

For signals within Band I and II, the direct RF sampling results for each of them are too many to be enumerated. Only GPS L1 C/A is taken to validate our design. For more specific results on the separation of different narrow band signals, please refer to [10] including the simulation of GPS L1/L2 and Compass-2 B1/B2/B3.

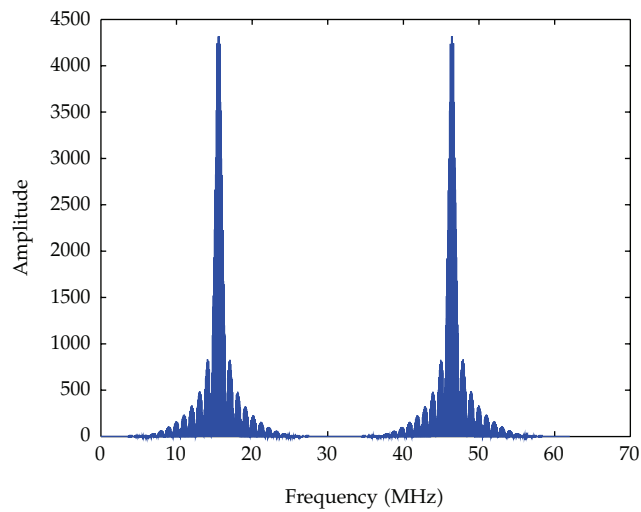
A piece of 4 ms data of GPS L1 C/A with no noise is generated at the clock rate of 744 MHz. From its spectrum shown in Figure 9, the carrier frequency 1575.42 MHz is down converted to its equivalent frequency: 87.42 MHz and 656.58 MHz.

Through the decimation and filtering network, the clock rate is lowered to 62 MHz. Then, having separated from Band II, GPS L1 baseband signal is upconverted to 15.58 MHz at the clock rate of 62 MHz. The spectrum is shown in Figure 10. The digital IF data is used by an FFT-based acquisition algorithm. Figure 11 shows a two-dimensional plot of the result.

A GPS L1 signal acquisition board is shown in Figure 12. Its ultimate sampling rate is 500 MHz. A set of about 6.9s data of true GPS L1 C/A signal with 1 bit quantization is



**Figure 9:** Signal spectrum of GPS L1 C/A at the sampling rate of 744 MHz.



**Figure 10:** Digital IF signal spectrum of GPS L1 C/A at the sampling rate of 62 MHz.

collected at the sampling rate of 372 MHz. It is used to validate the processing branch behind Module.1 in Figure 6. After processing, eight satellite signals can be acquired. Figure 13 shows the results of PRN10, PRN15, and PRN21.

## 6. Conclusions

In this paper, a scheme of the direct RF sampling at very high sampling rate is explored. The decimation and filtering network is designed to lower the sampling rate and complete the



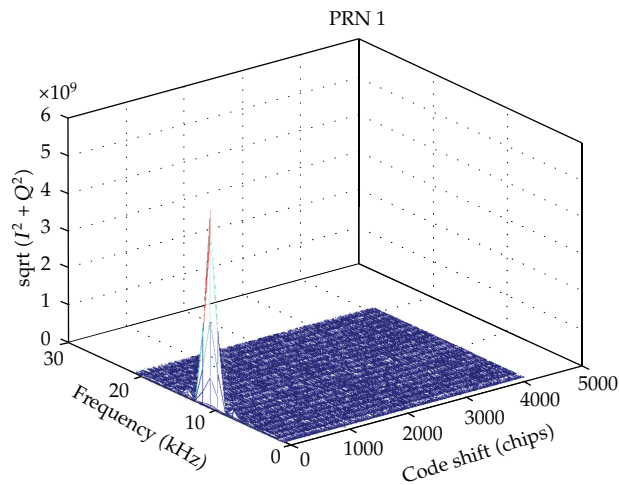


Figure 11: Correlation result for acquisition of GPS L1 C/A IF data at the sampling rate of 62 MHz.

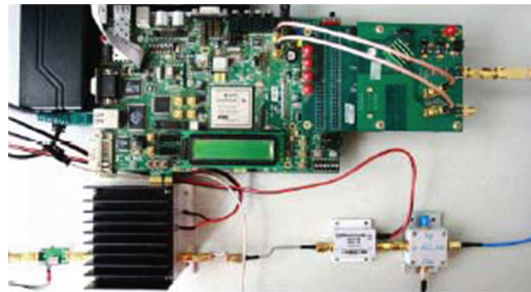


Figure 12: GPS L1 signal acquisition board [7].

down conversion of the target signal as well as its separation from others. As far as sampling Band I and II is concerned, the problem of keeping them from overlapping is solved by selecting proper sampling rate.

Experimental results show that the IF signal generated by the digitized RF front-end can be successfully acquired no matter in simulation or real environment, which verifies the scheme's feasibility. During the design of decimation and filtering network, multistage and efficient structures are applied, making it relatively easy for realization.

In all, the fully digitized RF front-end would offer significant advantages over the conventional design through the removal of analog-based hardware. With the advancement of ADCs and digital processors, it is predictable that the research on digitized RF front-ends will be much more attractive in future.

## Acknowledgments

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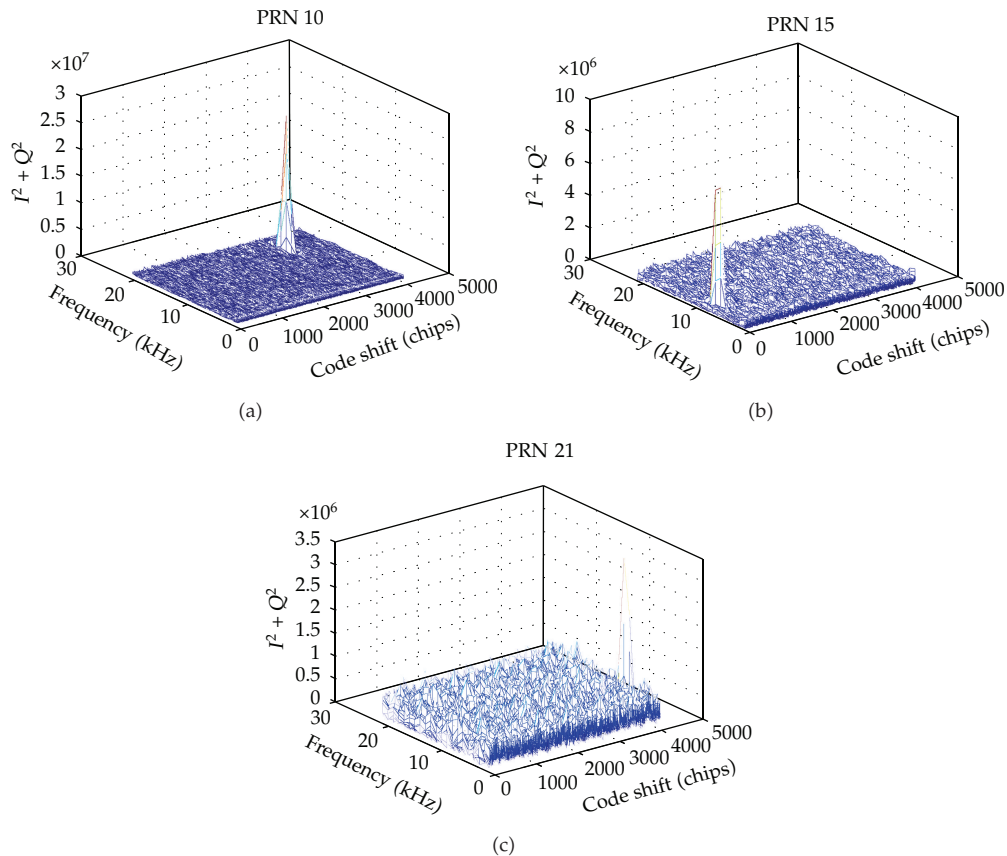


Figure 13: Correlation results for acquisition of PRN 10, 15 and 21.

and Development Program of China (863 Program) through Grants nos. 2007AA12Z336 and 2009AA12Z313. The authors gratefully thank Liu Hongquan of Beihang University for providing GPS signal acquisition board and collecting the data of the true GPS signal.

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